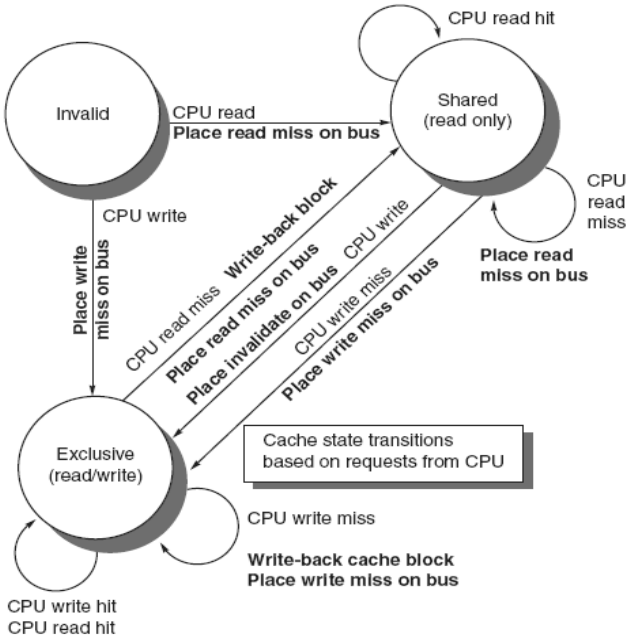
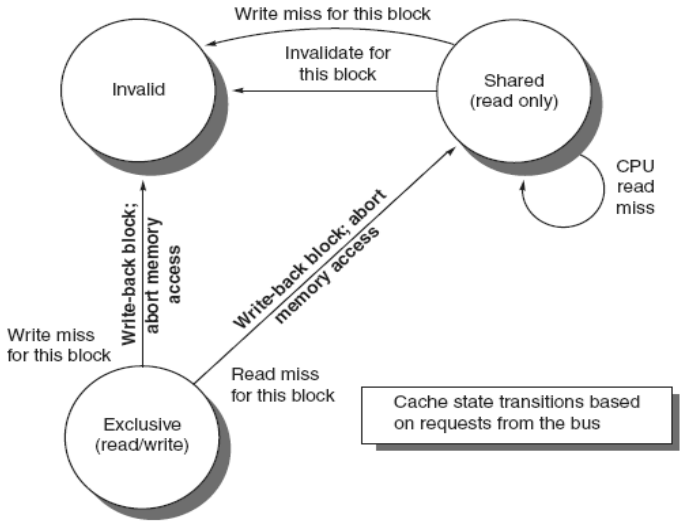
Exercise 1: Given a symmetric-memory multiprocessor based on the snooping bus protocol. Each processor has a private cache which is based on the MSI coherence protocol. Each cache line consists of a single word.





The following table shows the initial value in each cache of four different variables.

	Initial state			
Processor	**A**	**B**	**C**	**D**
P0	*Shared*	*Exclusive*	*Shared*	*Shared*
P1	*Invalid*	*Invalid*	*Invalid*	*Shared*
P2	*Invalid*	*Invalid*	*Shared*	*Shared*

The following table shows the final state of these variables after performing several memory accesses.

	Final state			
Processor	**A**	**B**	**C**	**D**
P0	*Invalid*	*Invalid*	*Invalid*	*Shared*
P1	*Invalid*	*Invalid*	*Shared*	*Exclusive*
P2	*Exclusive*	*Exclusive*	*Invalid*	*Shared*

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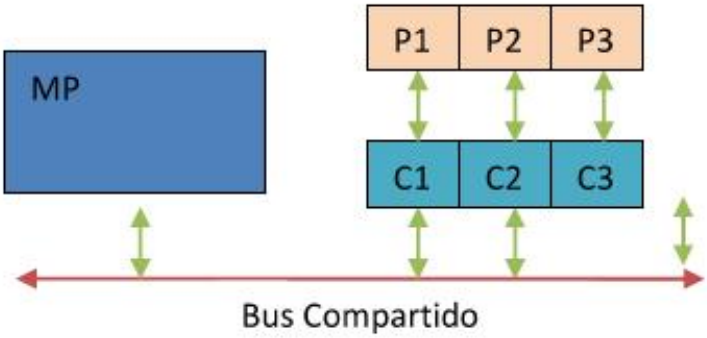
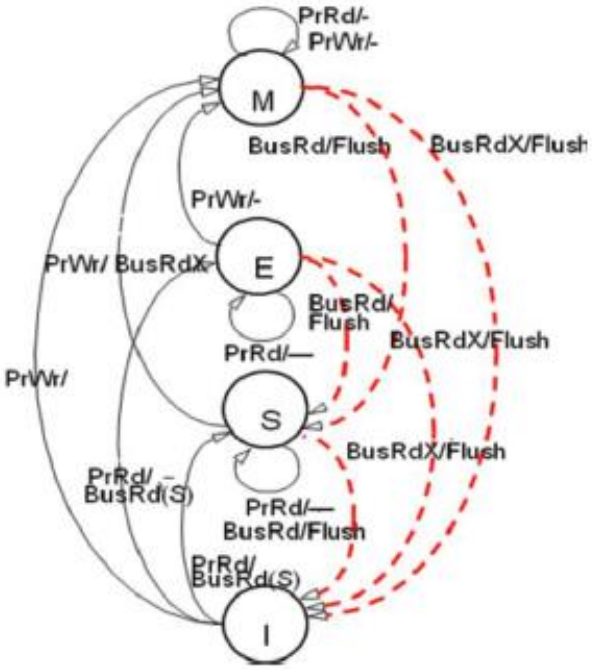
Complete the following tasks:

- Describe for each variable (A, B, C and D) what memory access/accesses are performed to reach the final state. Note 1: To reach the final state it could be necessary to perform a single or several memory accesses. Note 2: it is possible to have an unreachable final state (that is, a state without solution). Justify your answer.
- For each variable describe the generated bus traffic associated to the transition from the initial to the final state.

Exercise 2: Given a symmetric-memory multiprocessor based on the snooping bus protocol. Each processor has a private cache which is based on the MESI coherence protocol. All processers access the shared variables a, b and c.





Complete que following tables. Each one contains a sequence of memory accesses. Each sequence is independent and for all of them the cache memories are initially empty.

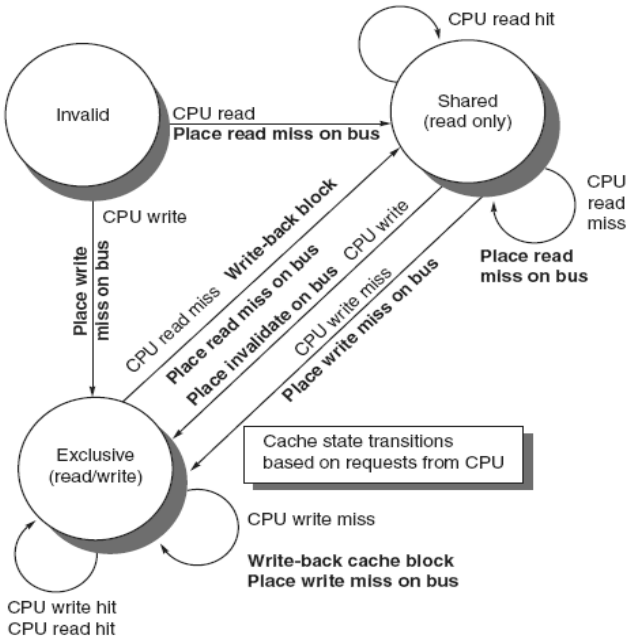
Action	Bus transition	Which provides the block? (M, C1, C2,C3)	Cache 1 state	Cache 2 state	Cache 3 state
P1-Read a					
P1-Write a					
P2-Read a					
P3-Write a					
P1-Read a					

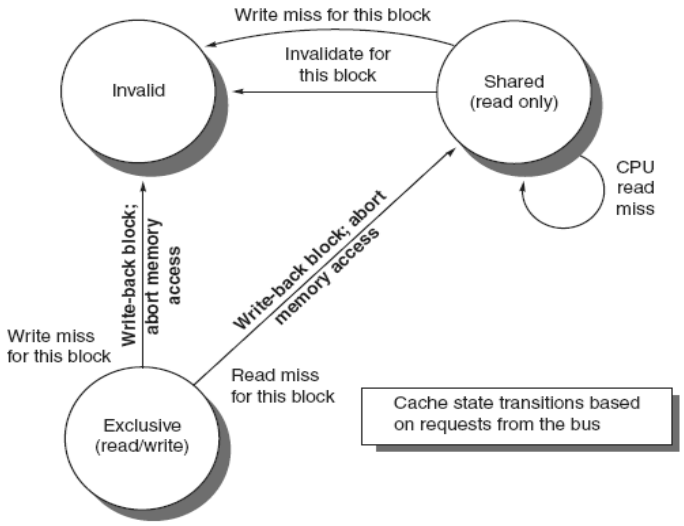
Action	Bus transition	Which provides the block? (M, C1, C2,C3)	Cache 1 state	Cache 2 state	Cache 3 state
P1-Read b					
P3-Read b					
P3-Write b					
P1-Read b					
P2-Read b					

Action	Bus transition	Which provides the block? (M, C1, C2,C3)	Cache 1 state	Cache 2 state	Cache 3 state
P2-Read c					
P2-Write c					
P2-Write c					
P3-Read c					
P1-Write c					

Exercise 3:

Given a symmetric shared memory system based on the snooping bus protocol and consisting of three processors. Each processor has a private cache based on the MSI protocol. The cache memories are direct-mapped and have only four cache lines with blocks of two words. Each cache uses the complete memory address of the block for the **tag field**.





The following tables show the initial state of each cache memory, with the least-significant word at the left.

Processor P0

Block	State	Tag	Data	
B0	I	0x00100700	0x00000000	0x7FAABB11
B1	S	0x00100708	0x00000000	0x00001234
B2	M	0x00100710	0x00000000	0x0077AABB
B3	I	0x00100718	0x00000000	0x7FAABB11

Processor P1

Block	State	Tag	Data	
B0	I	0x00100700	0x00000000	0x7FAABB11
B1	M	0x00100728	0x00000000	0xFF000000
B2	I	0x00100710	0x00000000	0xEEEE7777
B3	S	0x00100718	0x00000000	0x7FAABB11

Processor P2

Block	State	Tag	Data	
B0	S	0x00100720	0x00000000	0x1111AAAA
B1	S	0x00100708	0x00000000	0X00001234
B2	I	0x00100710	0x00000000	0x7FAABB11
B3	I	0x00100718	0x00001234	0x1111AABB

The following paragraphs are 3 different actions that have to be analyzed independently, all of them starting from the initial program state shown above.

a) P2: write 0x00100708, 0xFFFFFFFF
b) P2: read 0x00100708
c) P2: read 0x00100718

For each one the actions use a table like the one shown below. In each table show the changes that are produced in the cache memories. For the reads, write which will be the value read by the operation.

Processor	Block	Previous state	New State	Tag	Data	