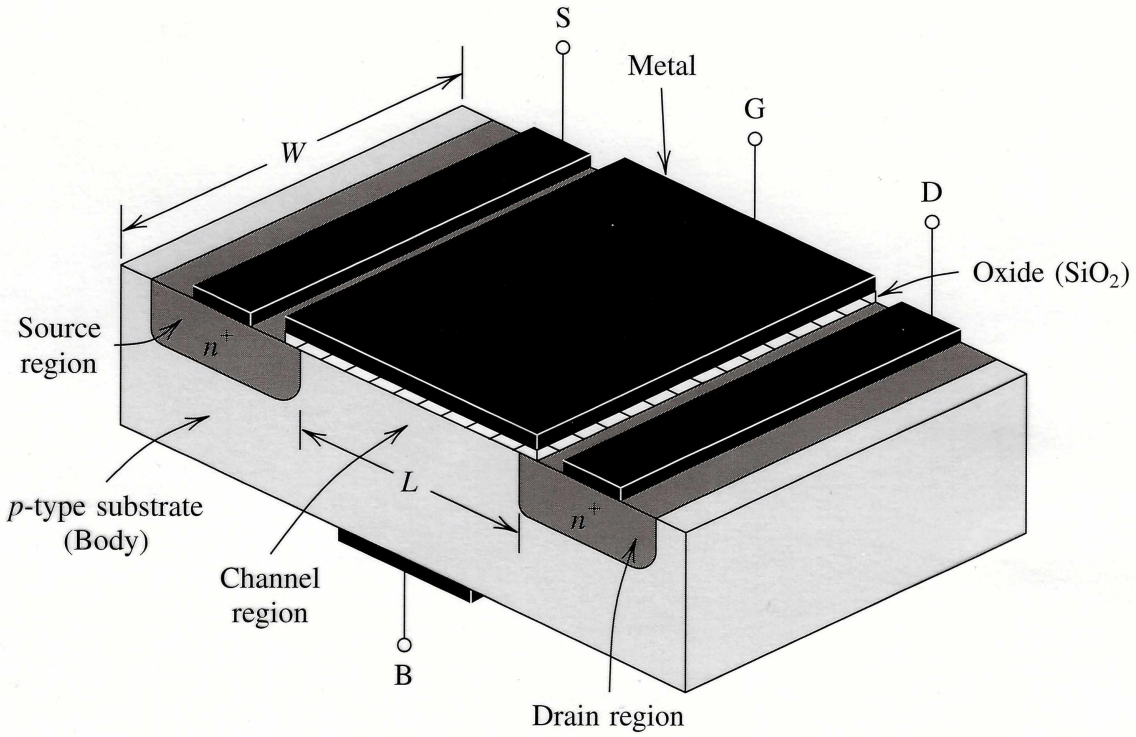
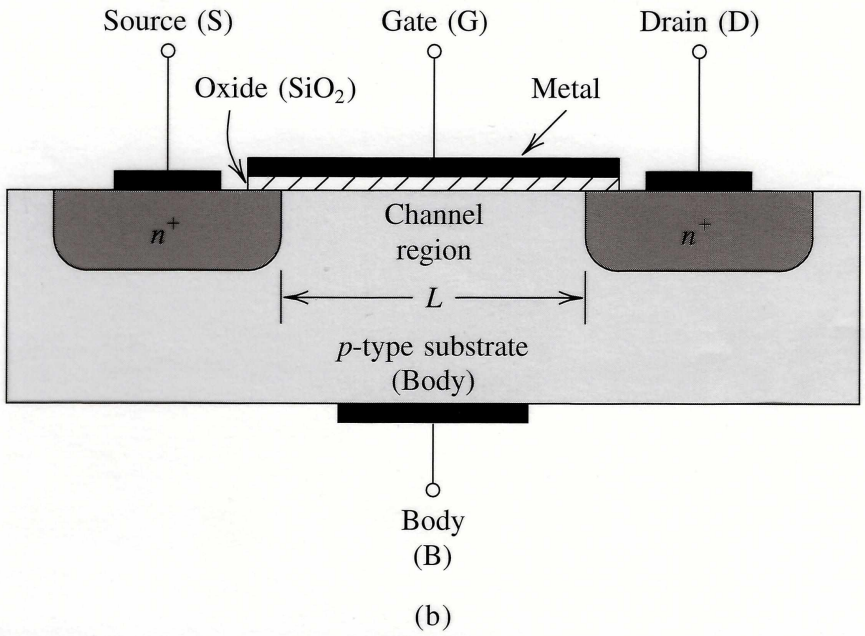


(a)



(b)

Fig. 5.1 Physical structure of the enhancement-type NMOS transistor: **(a)** perspective view; **(b)** cross section. Typically $L = 1$ to 10 μm, $W = 2$ to 500 μm, and the thickness of the oxide layer is in the range 0.02 to 0.1 μm.

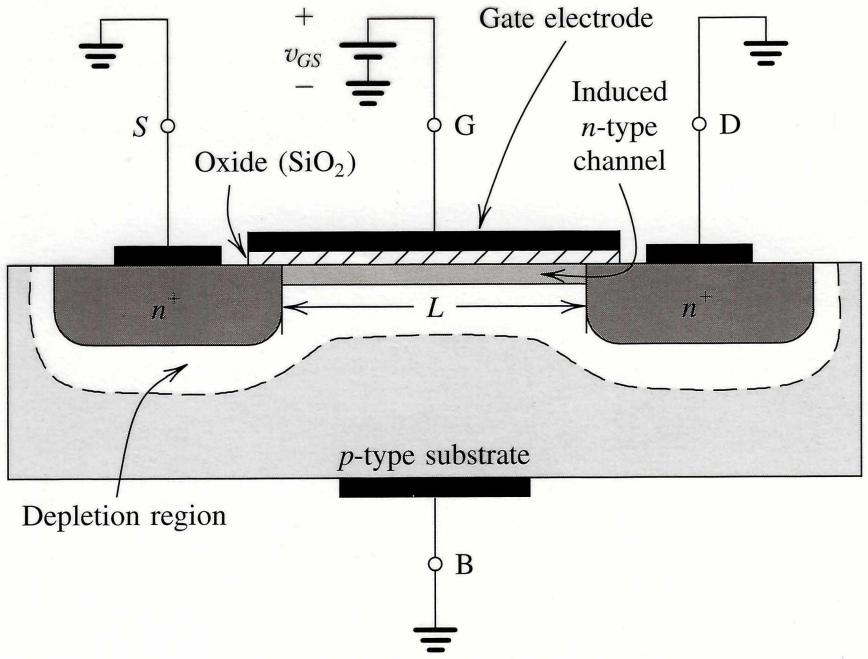


Fig. 5.2 The enhancement-type NMOS transistor with a positive voltage applied to the gate. An n channel is induced at the top of the substrate beneath the gate.

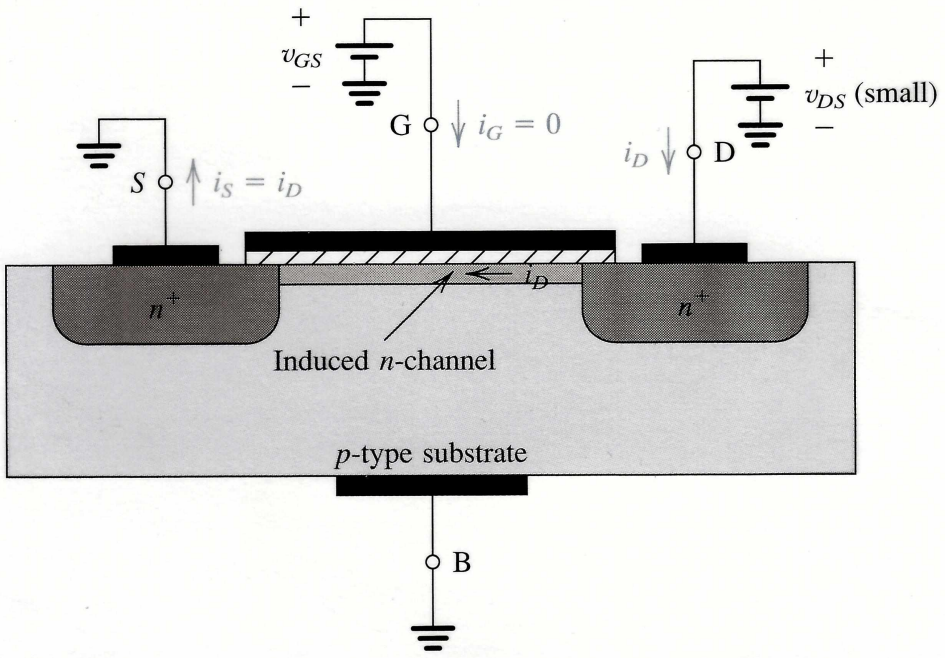


Fig. 5.3 An NMOS transistor with $v_{GS} > V_t$ and with a small v_{DS} applied. The device acts as a conductance whose value is determined by v_{GS}. Specifically, the channel conductance is proportional to $v_{GS} - V_t$, and thus i_D is proportional to $(v_{GS} - V_t)v_{DS}$. Note that the depletion region is not shown (for simplicity).

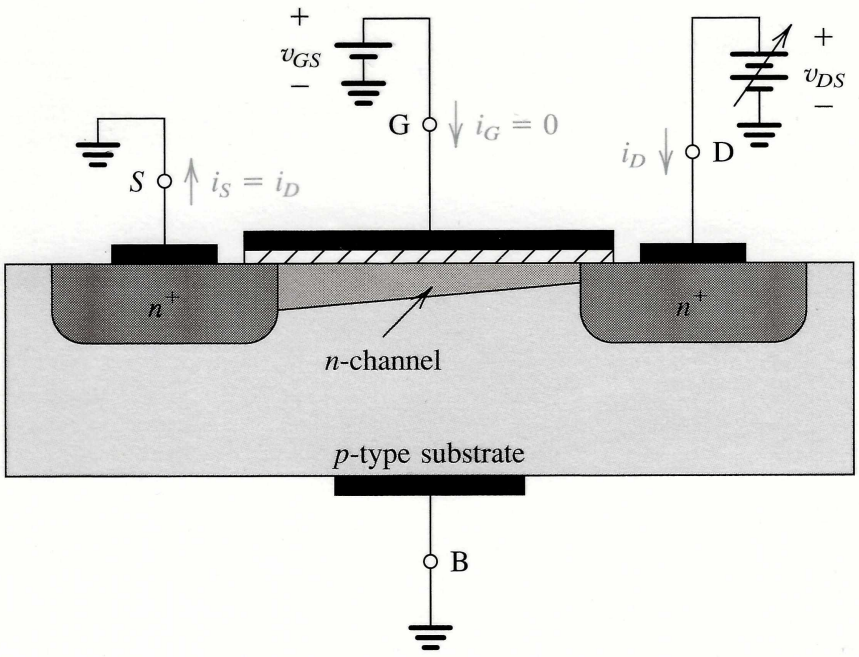


Fig. 5.5 Operation of the enhancement NMOS transistor as v_{DS} is increased. The induced channel acquires a tapered shape and its resistance increases as v_{DS} is increased. Here, v_{GS} is kept constant at a value $> V_t$.

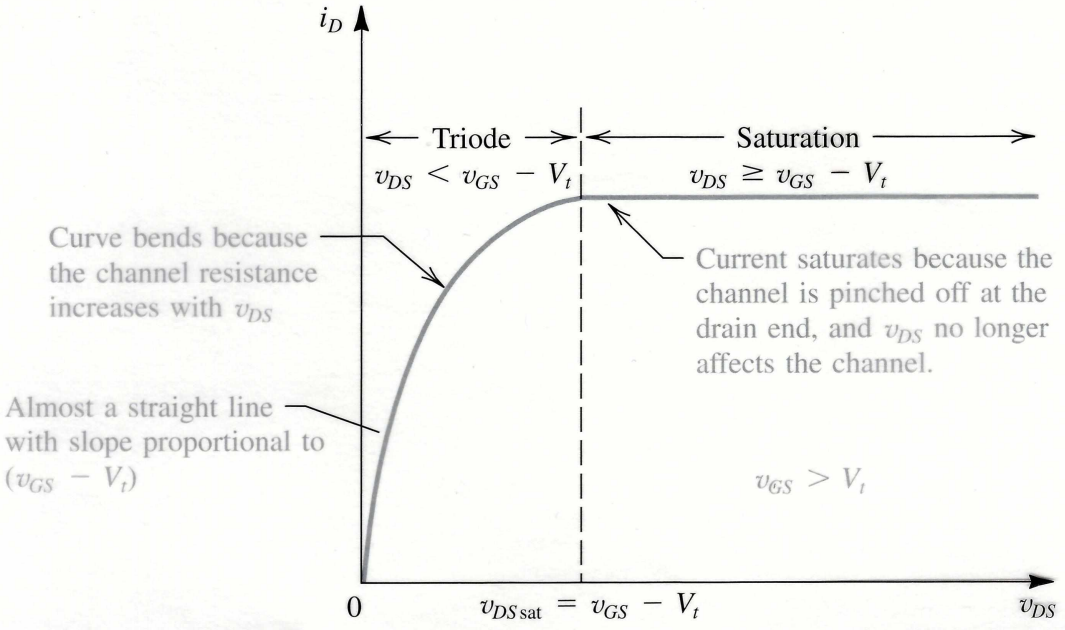


Fig. 5.6 The drain current i_D versus the drain-to-source voltage v_{DS} for an enhancement-type NMOS transistor operated with $v_{GS} > V_t$.

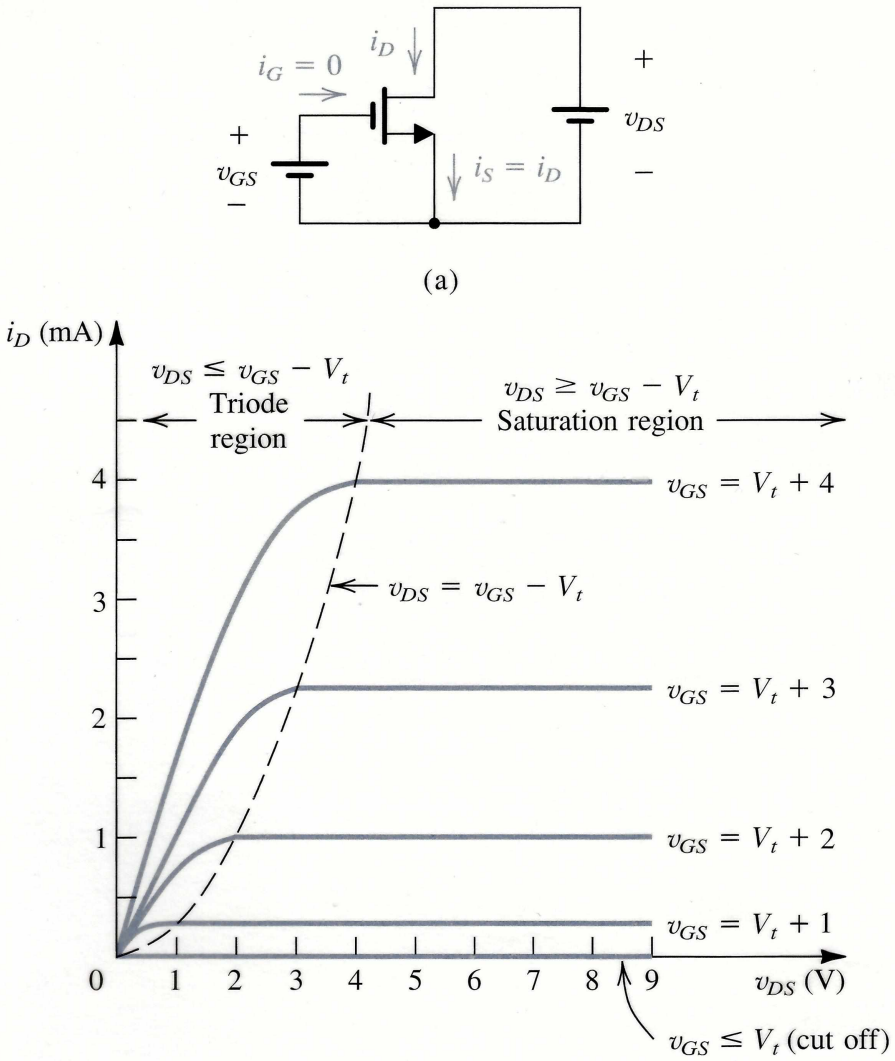


Fig. 5.11 **(a)** An *n*-channel enhancement-type MOSFET with v_{GS} and v_{DS} applied and with the normal directions of current flow indicated. **(b)** The i_D–v_{DS} characteristics for a device with $V_t = 1$ V and $k_n'(W/L) = 0.5$ mA/V^2.

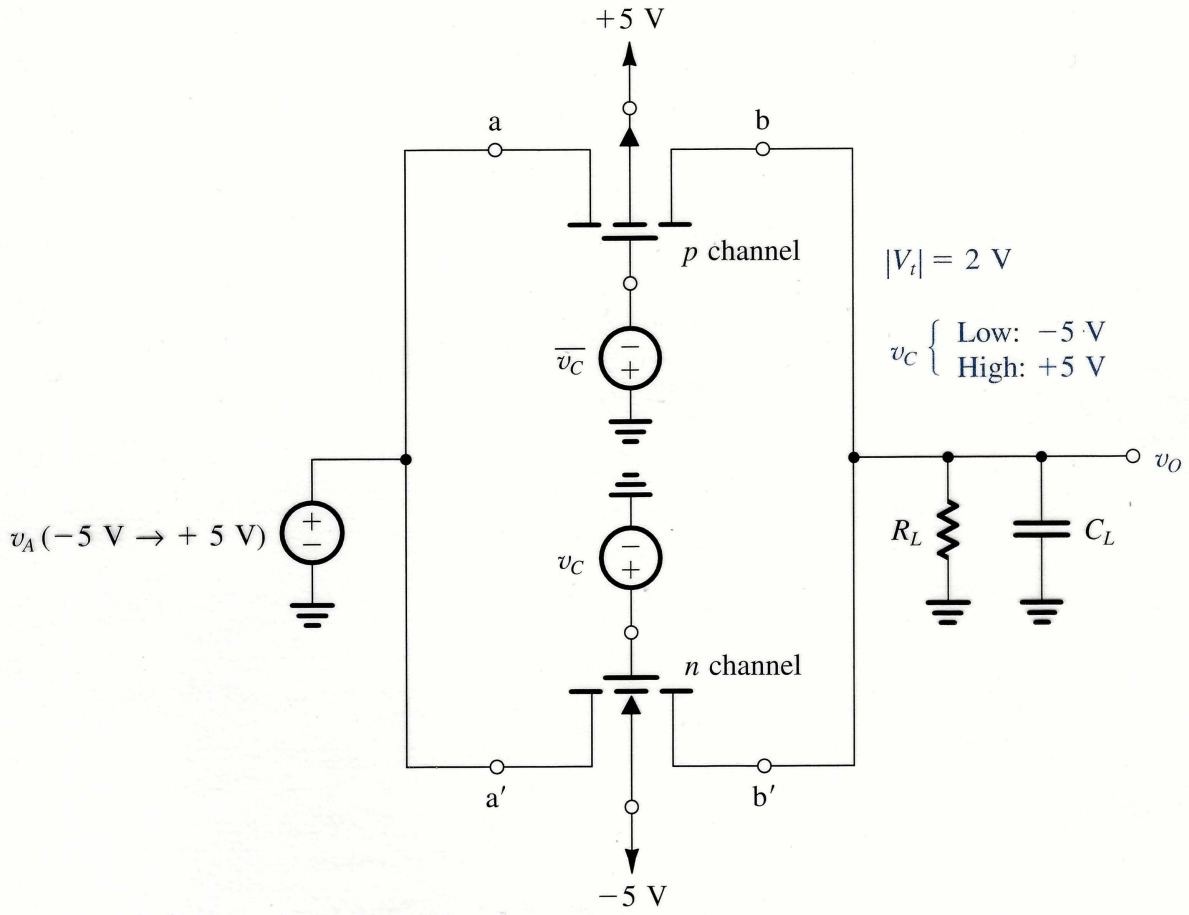


Fig. 5.64 The CMOS transmission gate.